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Authors that wish to refer to this work are advised to cite the full-length version by referring to its DOI:

https://doi.org/10.1002/jsid.647

High Temperature Thin-Film Barriers for Foldable AMOLED Displays

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ABSTRACT

We present a thin-film dual-layer bottom barrier on PI that is compatible with 350°C backplane processing for OLED displays. We demonstrate OLEDs that survive bending over 0.5 mm radius for 10.000x. Furthermore, we show compatibility of the bottom barrier with the backplane process by fabricating AMOLED displays on GEN1-sized substrates.

Keywords: High-temperature, thin-film barrier, foldable, AMOLED displays.

1. INTRODUCTION

OLED displays are extremely sensitive to degradation by the ambient. Moisture can enter through pinholes present in the electrodes or from the side of the pixels, leading to an oxidation of the cathode at the organic-cathode interface [1]. This causes a rapid formation of non-emissive regions in the device, so-called black spots, which are visible as single or clusters of dead pixels. Holst Centre has previously developed a thin-film encapsulation (TFE) for OLED devices on glass based on two inorganic layers of amorphous-hydrogenated silicon nitride (SiN) deposited by plasma-enhanced chemical vapor deposition (PECVD) separated by a thick organic coating for planarization (OCP) applied by inkjet printing [2,3]. The relatively thick organic OCP layer ensures decoupling of all pinholes present in both SiN layers. The longevity of protection against moisture relies on the low number of small pinholes in the SiN layers and a slow lateral transport in the OCP layer by means of a high sorptivity and low diffusivity in the organic material. Furthermore, the process temperature for the thin-film encapsulation is compatible with the underlying OLED device. A shelf life time of 20 years was demonstrated and the technology was transferred to production in 2014 for OLED lighting [3]. Due to the combination of high yield, low temperature processing, and excellent performance, comparable thin-film encapsulation stacks based on SiN/OCP/SiN can be found as top encapsulation in several AMOLED products on the market.

To fabricate flexible OLED lighting devices on plastic foil, the devices must be protected from the bottom side of the device and a thin film barrier needs to be applied on top of the substrate. Since fabrication of OLED lighting devices requires only a maximum temperature around 180°C, the same SiN/OCP/SiN stack used for top encapsulation was shown to be suitable as bottom barrier in flexible OLED lighting devices on PEN substrates [2].

For displays however, the temperature budget of the substrate and bottom barrier used for OLED lighting, is not sufficient. TFT backplane processes based on IGZO require temperature steps of 350 °C. As a consequence, instead of the cheaper alternatives PET or PEN, polyimide (PI) is used as a substrate in displays [4]. The previously developed Holst Centre thin film barrier stack of SiN/OCP/SiN is thermally stable up to 250°C and thereby not suitable in the bottom barrier of displays. In AMOLED display products this is resolved by the application of a thick (1-2 μm) inorganic barrier layer deposited by PECVD at high temperature. The inorganic layer is often a combination of SiO_2, SiN, and SiON layers to ensure a low pinhole density resulting in a high yield. Logically, since the thick inorganic bottom barrier consists of brittle layers, the flexibility of these devices is limited. A better solution in terms of yield and flexibility would be the use of thin inorganic layers in a dual-layer barrier stack comparable to the top encapsulation, but with a high temperature compatible organic interlayer (HT-OCP) which can be applied by spin coating or slot-die coating.

Here we investigate a thin-film (bottom) barrier stack comprising SiN/HT-OCP/SiN. Optical Ca tests and OLED black spot analysis are performed at accelerated climate conditions. By optimizing the layer thicknesses in the stack based on their mechanical and functional properties, we demonstrate foldable OLED devices fabricated on the high-temperature compatible substrate and barrier, and demonstrate no barrier damage after 10.000x folding over 0.5 mm radius. To show compatibility with AMOLED display processing we fabricated QQVGA 100 ppi monochrome AMOLED displays on top of the high-temperature bottom barrier.

2. BOTTOM BARRIER PERFORMANCE

Since the thin-film encapsulation developed at Holst Centre was demonstrated to be suitable for long life time OLED products, the top barrier serves as an excellent performance reference for a new high temperature compatible bottom barrier for display. The barrier performance is determined by a combination of factors: the intrinsic water vapor transmission rate (WVTR) of the SiN (I), the number and size of the pinholes in SiN (which can be quantified as an extrinsic WVTR; the amount of water entering solely through pinholes) (II), the rate of lateral spreading of water in the organic interlayer (III), and (IV) the combined performance when present in a stack of SiN/HT-OCP/SiN. Each of these factors will be determined using a different experimental testbed.

I - Intrinsic water vapor transmission rate

For determining low-value intrinsic barrier properties of the SiN layers, the optical Ca-test developed at Philips Research has been shown to be an accurate test configuration [5]. By looking at the gradual uniform increase in transmission of semi-transparent metallic Ca films upon exposure to air, WVTR values as low as 10^{-6} g/m^2/day can be determined. To measure the intrinsic properties of the first SiN layer deposited at 350 °C by PECVD, we deposited 40 nm Ca on top of PI/SiN and we encapsulated the Ca with a multi-layer thin film barrier of which the properties are known. The test was performed at accelerated conditions of 60°C and 90% relative humidity (hereafter abbreviated to 60/90). The uniform Ca degradation is determined from the slope of calcium thickness in time, see Fig. 1. The intrinsic WVTR was determined to be 6×10^{-6} g/m^2/day at 60/90, corresponding to a value of $WVTR_{int}$ around 3×10^{-7} g/m^2/day at 20/50, when we use a conservative acceleration factor of 20.

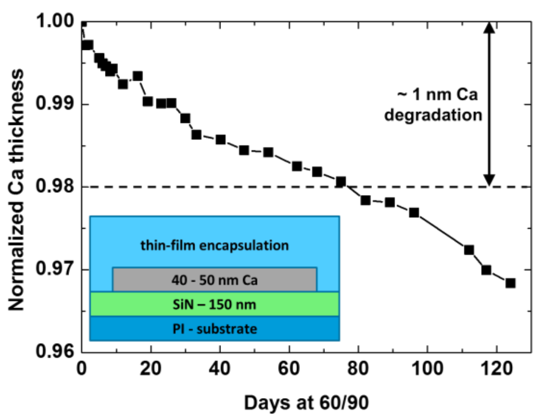

Fig. 1. Ca degradation monitored in time at 60/90 for determination of intrinsic WVTR.

II - Extrinsic water vapor transmission rate

To obtain a reliable value for extrinsic WVTR, we performed a similar experiment as for intrinsic WVTR, but where the metallic Ca is replaced by an organic with dispersed water-sensitive nanoparticles. When the nanoparticles react with water, so-called saturated spots appear from which the total amount of water can be determined. This method is ideal for layers with low pinhole density since it is relatively easy to measure over large areas. Fig. 2 shows schematically the test configuration and a photograph (right) of the water sensitive layer after exposure for 306h to 60/90. The area photographed is 14x14 cm. The detailed image clearly shows the small saturated spots. We obtain an extrinsic WVTR of 3×10^{-5} g/m^2/day at 60/90, corresponding to 1.5×10^{-6} g/m^2/day at 20/50 conditions. The total WVTR of the SiN is determined by the combination of intrinsic and extrinsic characteristics, and in this case the total WVTR is dominated by the extrinsic results. A total WVTR of 10^{-6} g/m^2/day is very comparable to that obtained on SiN layers used in the reference thin film top encapsulation.

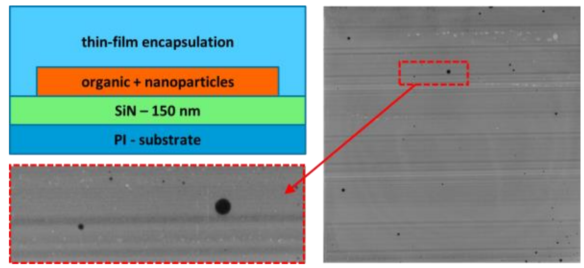

Fig. 2. Photographs of saturated spots in a test area of 14x14 cm (right) used to determine the extrinsic WVTR..

III - Lateral spreading of water in the organic

To measure the rate of lateral spreading of water in the organic interlayer, which determines the time that it takes for water to migrate from a pinhole in the first SiN layer to a pinhole in the second SiN layer, we performed side leakage measurements on HT-OCP according to previously described method where laser slits are made at a variable distance from a Ca-pad and the time to Ca degradation is monitored [6]. The results are shown in Fig. 3 where the side leakage distance in HT-OCP is plotted versus time at 60/90. For comparison a graph of OCP from the best performing TFE was added. Both materials show the expected square-root of time behavior. Clearly, the lateral transport is much slower in HT-OCP compared to low temperature OCP, indicating a very low diffusion coefficient for HT-OCP. The difference in time for comparable side leakage distance is about a factor of 6.

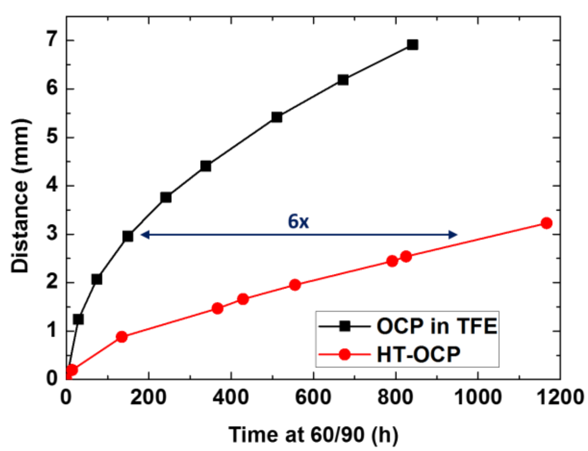

Fig. 3. Side leakage distance plotted in time at 60/90. OCP from best TFE stack is added as a reference. Clearly the HT-OCP has a lower lateral spreading rate of water compared to the OCP used in the top encapsulation of OLED devices.

IV - Complete barrier stack performance

We measured the total barrier stack performance by 2 methods: 1) by using 40 nm thick Ca-pads and 2) by using encapsulated flexible OLED devices. For both experiments the depositions were performed on top of PI substrates with the high temperature barrier stack present and experiments were performed at 60/90 conditions. The results are shown in Fig. 4A and 4B. In the case of Ca-pads, we monitor the number of Ca pads that develop so-called white spots (the transparent area where water reacts with Ca to $Ca(OH)_2$. This is shown in Fig. 4A. Here we compare the number of Ca-pads without white spots for a single SiN layer, and we have two curves for a full barrier stack; one fabricated at the research PECVD tool for 6-inch plates, and one fabricated at the GEN1 pilot line facility. The single SiN layer shows a rapid increase in the number of white spots and for both full barrier stacks all Ca-pads remain completely intact for 150 days at 60/90. For OLEDs we monitor the formation of back spots in time. Fig. 4B shows a photograph of the emission of an OLED (~8 cm^2) after exposure to 60/90 for 667 hours. No black spots are observed. In general, for the devices tested we did not obtain any visible black spots due to water ingress through the bottom barrier after a duration of 500h at 60/90. The OLED as a testbeds is more sensitive compared to the Ca-test since only a few nm of cathode oxidation thickness is sufficient to completely block electron injection into the organic layers.

3. FOLDABLE OLED DEVICES

To achieve ultra-flexible or foldable encapsulated OLED devices, the complete stack of substrate, top- and bottom barrier, and device needs to be optimized from mechanical performance. We used a multi-layer model (which has as input the layer thickness and Youngs modulus of each layer) to determine the neutral line in the stack and the strain levels in the outer SiN layers at different bending radii. An example is shown in Fig. 5, where the strain of a fully encapsulated OLED device on PI is given at 2mm

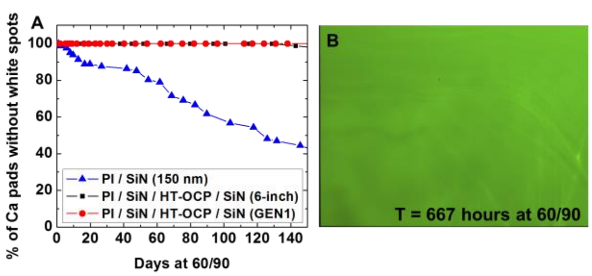

Fig. 4. (A) Monitoring of white spots in Ca-pads in time at 60/90. (B) Photograph of an OLED on top of PI with high temperature bottom barrier, after exposure to 60/90 for 667h. For both cases, no white spots (Ca) or black spots (OLED) were present in the devices during test.

bending radius. The outer SiN layer locations are depicted by dotted red lines and labelled SiN 1 (first SiN in high temperature bottom barrier) and SiN 4 (last SiN layer in top encapsulation). As can be seen from the graph, when the topcoat, OCP, HT-OCP, and PI thicknesses are tuned, the neutral line can be very close to the device and at 2mm bending radius the outer SiN layers experience a strain much lower than their failure strain around 0.8%.

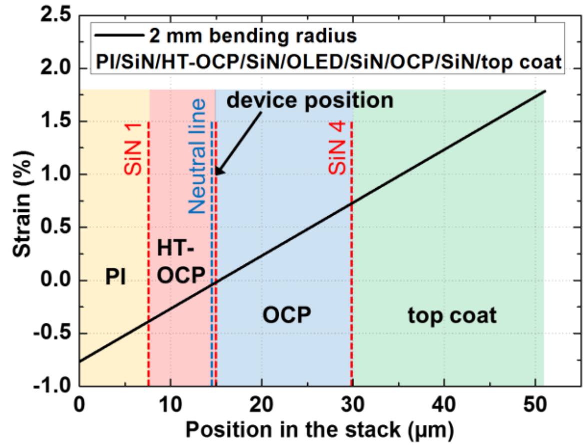

Fig. 5. The failure strain as a function of position in a fully encapsulated OLED stack, at a bending radius of 2mm. The neutral line is close to the device and the outer SiN layers experience strain levels below the failure strain.

To demonstrate that encapsulated OLEDs on high temperature barrier can survive repetitive bending at small radii, we fabricated different stacks for bottom barrier with varying PI-substrate and HT-OCP thicknesses, in combination with a varying TFE. For the thicknesses of the layers shown in Fig. 5, OLEDs were fabricated and the results are shown in Fig. 6. Here a blue solution processed OLED on top of the high temperature bottom barrier is shown in bended condition with a bending radius of 0.5 mm. Fig. 6B shows a photograph of the emission of a small molecule evaporated OLED device, directly after fabrication and after 985h at 60/90. Prior to the accelerated climate testing, the device was bent over different radii for 10.000x. The locations where the bending was performed over 0.5 and 1 mm radius are indicated by the dotted lines and by the arrows. After 10.000x bending over 0.5 mm radius, no damage is observed after extensive 60/90 testing. To find the limits in bending radius, bending over 0.25 mm radius was also performed. The results after 60/90 are shown in the right figure in Fig. 6B. A clear dark line has appeared surrounded with clusters of black spots, indicating barrier failure at a bending radius < 0.5 mm.

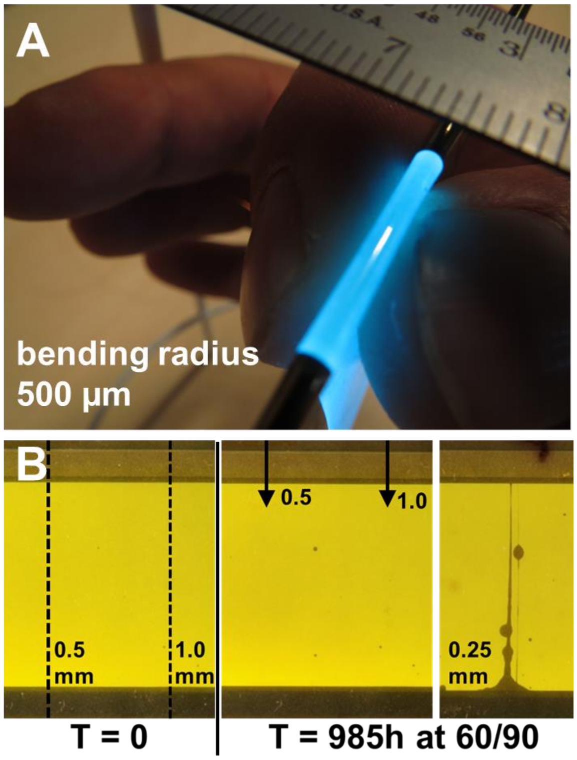

Fig. 6. (A). A solution processed OLED bent over a 0.5 mm radius. (B) Accelerate life time test of OLEDs that were bent 10.000x over different bending radius.

4. AMOLED DISPLAY COMPATIBILITY

To demonstrate the compatibility of the high-temperature barrier on PI with the AMOLED display processing on top, in particular with the (oxide) TFT backplane processes, we realized a QQVGA 100 ppi display. On top of PI substrates with the developed barrier stack, a 350 °C self-aligned IGZO TFT backplane. OLED frontplane and Holst Centre TFE were deposited. An image loaded on the resulting QQVGA 100 ppi display is shown in Fig. 7, clearly demonstrating the compatibility of the thin film bottom barrier stack with AMOLED display processes.

5. CONCLUSIONS

We have developed a thin-film bottom barrier stack where two thin SiN layers are separated by a thicker organic layer that is 350 °C high-temperature stable. The SiN/HT-OCP/SiN stack was shown to be suitable for AMOLED display processing. By optimizing the mechanical properties of the complete stack, foldable devices can be fabricated with bending radii as small as 500 µm.

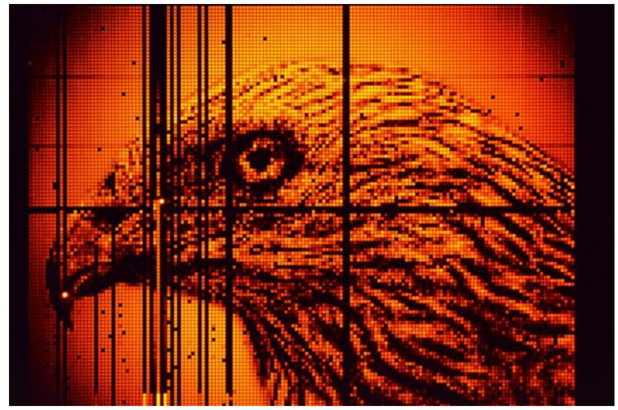

Fig. 7. Photograph of a loaded image to the QQ VGA AMOLED display on top of the high-temperature SiN/HT-OCP/SiN bottom barrier.

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ACKNOWLEDGEMENTS

The authors would like to thank colleagues of Holst Centre's GEN1 TFT Pilot Line for their work on the IGZO backplanes

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